What is claimed is:

1. A semiconductor device comprising:

a substrate which has a chip region and a pad region which is in a periphery of the chip region;

a semiconductor chip which is located on the chip region and includes an electrode pad which is formed thereon;

a conductive pad which is placed on the pad region;

a first wall which is arranged in the pad region;

a second wall which is arranged on the semiconductor chip and faces towards the first wall;

a conductive line which electrically connects the electrode pad with the conductive pad and is arranged between the first wall and the second wall;

an encapsulating material which encapsulates the conductive element and is contained between the first and second walls.

2. The semiconductor device according to claim 1, wherein the pad region surrounds the chip region, and wherein the semiconductor device further

comprises:

a plurality electrode pads which are located along an edge of the semiconductor chip;

a plurality of conductive pads which are placed on the pad region and correspondent with the plurality of electrode pads; and

a plurality of conductive lines which electrically connect the plurality of electrode pads with the conductive pads and are arranged between the first wall and the second wall;

wherein the first wall surrounds the chip region;

wherein the second wall covers a middle of the semiconductor chip; and

wherein the encapsulating material encapsulates the plurality of conductive lines.

3. The semiconductor device according to claim 2, wherein a configuration of the semiconductor device is a rectangle, wherein the plurality of electrode pads are respectively arranged on each edge of the rectangle, and wherein the conductive pads are respectively arranged as to correspond with the electrode

pads.

4. The semiconductor device according to claim 3, wherein the first wall is a frame which surrounds the chip region.

5. The semiconductor device according to claim 1, wherein the substrate has a central concave portion and the semiconductor chip is mounted in the concave portion.

6. The semiconductor device according to claim 1, wherein a surface of the semiconductor chip is covered by the second wall and the encapsulating material.

7. The semiconductor device according to claim 6, wherein the encapsulating material is a resin.

8. The semiconductor device according to claim 1, wherein the second wall has a upper surface and a lower surface which contacts the semiconductor chip, wherein the upper surface is higher than the conductive line and wider than the lower surface.

9. The semiconductor device according to claim 3, wherein the second wall has a upper surface and a lower surface which contacts to the semiconductor chip,

wherein the upper surface is higher than the conductive lines and wider than the lower surface.

10. The semiconductor device according to claim 9, wherein each distance between each conductive lines and the second wall is substantially regular.

11. The semiconductor device according to claim 2, wherein a substantially planar surface is formed by upper surfaces of the first and second walls and the encapsulating material.

12. A method for fabricating a semiconductor device comprising:

providing a substrate which has a chip region and a pad region which is in the periphery of the chip region;

placing plural conductive pads on the pad region;

mounting a semiconductor chip on the chip region, wherein the semiconductor chip includes a plurality of electrode pads which are formed thereon;

connecting conductive lines between the electrode pads and the conductive pads;

forming a first wall in the pad region;

forming a second wall on the semiconductor chip so as to face to the first wall, such that the conductive lines are arranged between the first and second walls; and

supplying an encapsulating material into a space between the first and second walls so as to encapsulate the conductive lines.

13. The method according to claim 12, further comprising

shaving a top surface of the second wall after supplying the encapsulating material.

14. The method according to claim 12, wherein a concave portion is located in the chip portion, and wherein the semiconductor chip is mounted in the concave portion.

15. A method for fabricating a semiconductor device comprising:

providing a substrate which has a chip region and a pad region which is in the periphery of the chip region;

placing plural conductive pads on the pad region;

mounting a semiconductor chip on the chip region, wherein the semiconductor chip includes a plurality of electrode pads which are formed thereon;

connecting the electrode pads with the conductive pads by conductive lines;

forming a first wall in the pad region;

placing a cover above the chip region, wherein the cover includes an open portion for introduction of an encapsulating material; and

introducing the encapsulating material into a space between the cover and the chip region through the open portion so as to encapsulate a surface of the semiconductor chip and the conductive lines.

16. The method according to claim 15, wherein the cover has a upper surface and lower surface which faces to the chip region, wherein a release agent is formed on the lower surface before introducing the encapsulating material.

17. The method according to claim 15, wherein the cover is a lattice structure, and wherein grids of the cover is placed so as to extend to an upper of

the conductive lines.

18. The method according to claim 15, wherein the first wall surrounds the chip region, and wherein an area of the cover is less than an area which is surrounded by the first wall.

19. The method according to claim 15, wherein the cover includes a second open portion which exhausts a gas in a space between the chip region and the cover while introducing the encapsulating material.

20. The method according to claim 15, wherein the gas is exhausted by an aspirator.